REMARKS

In the Office Action[1] mailed August 30, 2006, the Examiner rejected claims 1, 10, 12, 14, 15, 17 under 35 U.S.C. § 112, second paragraph, as being indefinite; rejected claims 1-3 under 35 U.S.C. § 102(e) as being anticipated by Pate (U.S. Patent Application Publication No. 2004/0080717, hereafter "Pate"); and rejected claims 3-23 under 35 U.S.C. § 103(a) as being unpatentable over Pate in view of Maitra (U.S. Patent No. 5,623,647, hereafter "Maitra").

With this response, Applicant has amended claims 1, 4, 9, 14, 15, and 19 to further clarify the scope of the original claims only and not to narrow the scope of any claim. No claims have been canceled. Accordingly, claims 1-23 remain pending.

I. Rejection of claims 1, 10, 12, 14, 15, 17 under 35 U.S.C. § 112, second paragraph:

Applicant respectfully traverses the rejection of claims 1, 10, 12, 14, 15, and 17 under 35 U.S.C. § 112, second paragraph, as being indefinite. However, to expedite prosecution, Applicant has amended claims 1, 9, 14, and 15 with respect to antecedent basis for the element of "the chip," as recited in claims 1, 10, 12, 14, 15, and 17, and the element of "the temperature range," as recited in claim 15. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 1, 10, 12, 14, 15, and 17 under 35 U.S.C. § 112, second paragraph.

[1] The Office Action may contain statements characterizing the related art, case law, and claims. Regardless of whether any such statements are specifically identified herein, Applicant declines to automatically subscribe to any statements in the Office Action.

II. Rejection of claims 1-3 under 35 U.S.C. § 102(e):

Applicant respectfully traverses the rejections of claims 1-3 under 35 U.S.C. § 102(e) as being anticipated by Pate. In order to properly establish that Pate anticipates Applicant's claimed invention under 35 U.S.C. § 102, each and every element of the claims in issue must be found, either expressly described or under principles of inherency, in that single reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." See M.P.E.P. § 2131, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Claim 1, as amended, recites a method comprising "monitoring one or more sensor outputs measuring a power consumption property of a chip," (emphasis added). Pate fails to teach at least this element.

The Examiner asserted, "[a]s per claim 1, Pate teaches the invention comprising: ... the sensor to measure a power consumption property [where the sensor 610 senses the temperature] of the chip," Office Action at pages 3-4. However, this is incorrect.

Pate discloses in paragraph [0036], "[t]he mechanism 610 thus senses the temperature of the light source 604 of the assembly 603," (emphasis added). Accordingly, Pate fails to teach or suggest "a power consumption property of a chip," as recited in claim 1.

For at least this reason, Pate fails to teach each and every element of claim 1, and cannot anticipate claim 1. Claim 1 is allowable. Claims 2-3 depend from claim 1, and are thus also allowable at least due to their dependence. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 1-3 under 35 U.S.C. § 102(e).

III. Rejection of claims 3-23 under 35 U.S.C. § 103(a):

Applicant respectfully traverses the rejection of claims 3-23 under 35 U.S.C. § 103(a) as being unpatentable over Pate in view of Maitra. A *prima facie* case of obviousness has not been established.

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). M.P.E.P. § 2142, 8th Ed., Rev. 2 (May 2004), p. 2100-128.

A *prima facie* case of obviousness has not been established because, among other things, neither Pate, nor Maitra, nor their combination, teaches or suggests each and every element of Applicant's independent claims.

Claims 3-5 depend from claim 1, and thus includes every element of claim 1. As set forth above, Pate fails to teach at least "measuring a power consumption property of a chip," as recited in claim 1, and recited by dependent claims 3-5. However, in rejecting claims 3-5 under 35 U.S.C. § 103(a), the Examiner further cited Maitra, but failed to notify Applicant the reasons for rejection. In accordance with the patent statue, "Whenever, on examination, any claim for a patent is rejected, or any objection ... made," notification of the reasons for rejection and/or objection together with such information and references as may be useful in judging the propriety of continuing the prosecution (35 U.S.C. 132) should be given. See M.P.E.P. § 707. For at least this

reason, the rejection of claims 3-5 under 35 U.S.C. § 103(a) as being unpatentable over Pate in view of Maitra is improper, and should be withdrawn.

With respect to claim 6, the Examiner acknowledges "Pate does not teach ... correlating the event data with that of the application," Office Action at page 5. However, the Examiner asserts in the Office Action at pages 5-6, "Maitra teaches ... correlat[ing] the event data with the application [Col 8 line 55 - Col 9 line 1; the amount of time required for each application is correlated with the next application to be run]." The Examiner's assertion is incorrect.

Maitra, in column 8, lines 53-58, discloses the following:

> Next, the clock scheduling unit determines the scheduled application to be run by the microprocessor in the next quantum. Typically, the clock scheduling unit accesses this information from a task scheduling unit which prioritizes each application and determines the amount of CPU time each application receives. (Emphasis added).

However, determining the scheduled application to be run by the microprocessor, and determining the amount of CPU time each application receives, as taught by Maitra, does not constitute "correlating the event data with the parts of the application," where the event data "include[s] times that one or more sensor outputs indicates the existence of a power consumption property of a chip," as recited in claim 6. Therefore, Pate and Maitra, taken either alone, or in any reasonable combination, fail to teach or suggest each and every element of independent claim 6.

For at least this reason, Pate and Maitra fail to establish a *prima facie* case of obviousness. Claim 6 is allowable. Independent claims 9, 14, and 19, while of different scope than claim 6, recite claim limitations similar to those of claim 6. Accordingly, claims 9, 14, and 19 are allowable at least due to the same reasons set forth above.

Further, claims 7-8, 10-13, 15-18, and 20-23 depend respectively from claims 6, 9, 14, and 19, and are also allowable at least due to their dependence. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 3-23 under 35 U.S.C. § 103(a).

IV. Conclusion:

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration of this application and timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

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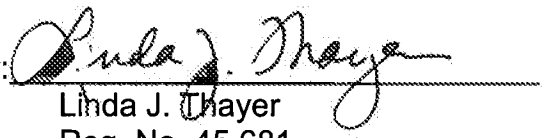
By: 
Linda J. Thayer
Reg. No. 45,681